

Substitute for Form 1449 A &amp; B/PTO

# **INFORMATION DISCLOSURE STATEMENT BY APPLICANT**

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Sheet

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of

2

Complete if Known

Application Number	09/805,899
Confirmation Number	3488
Filing Date	March 15, 2001
First Named Inventor	Seongmoon WANG
Art Unit	2133
Examiner Name	Shelly A. CHASE
Attorney Docket Number	A7936

## **U.S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
		Number	Kind Code <sup>2</sup> (if known)		

## **FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Translation <sup>6</sup>
		Country Code <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (if known)			

## **NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city, and/or country where published.	Technology Center 2100 Translation <sup>6</sup>
SAC		M. Abramovici, M. A. Breuer, and A. D. Friedman. <i>Digital Systems Testing and Testable Design</i> . Computer Science Press, New York, N.Y., 1990.	
SAC		M. F. AlShaibi and C. R. Kime. MFBIST: A BIST Method for Random Pattern Resistant Circuits. In <i>Proceedings IEEE International Test Conference</i> , pages 176-185, 1996.	
SAC		M. Bershteyn. Calculation of Multiple Sets of Weights for Weighted Random Testing. In <i>Proceedings IEEE International Test Conference</i> , pages 1031-1040, 1993.	
SAC		P. H. B., W. H. McAnney, and J. Savir. <i>Built-In Test for VLSI: Pseudorandom Techniques</i> . John Wiley & Sons, 1987.	
SAC		D. E. Goldberg. <i>Genetic Algorithms in Search, Optimization, and Machine Learning</i> . Addison Wesley, Reading, M.A., 1989.	
SAC		J. Hartmann and G. Kemnitz. How to Do Weighted Random Testing for BIST. In <i>Proceedings IEEE International Conference on Computer-Aided Design</i> , pages 568-571, 1993.	
SAC		J. H. Holland. <i>Adaptation in Natural and Artificial Systems</i> . University of Michigan Press, Ann Arbor, M.I., 1975.	
SAC		M. Karkala, N A. Touba, and H.-J. Wunderlich. Special ATPG to Correlate Test Patterns for Low-Overhead Mixed-Mode BIST. In <i>In proceedings 7rd Asian Test Symposium</i> , 1998.	
SAC		S. Pateras and J. Rajski. Cube-Contained Random Patterns and Their Application to the Complete Testing of Synthesized Multi-level Circuits. In <i>Proceedings IEEE International Test Conference</i> , pages 473-482, 1991.	
SAC		I. Pomeranz and S. Reddy. 3-Weight Pseudo-Random Test Generation Based on a Deterministic Test Set for Combinational and Sequential Circuits. <i>IEEE Trans. On Computer-Aided Design of Integrated Circuit and System</i> , Vol. 12:1050-1058, July 1993.	
SAC		N. Touba and E. McCluskey. Synthesis of Mapping Logic for Generating Trans-formed Pseudo-Random Patterns for BIST. In <i>Proceedings IEEE International Test Conference</i> , pages 674-682, 1995.	
SAC		N. A. Touba and E. J. McCluskey. Altering a Pseudo-Random Bit Sequence for Scan-Based BIST. In <i>Proceedings IEEE International Test Conference</i> , pages 167-175, 1996.	

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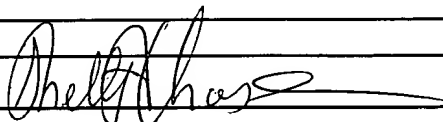
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S-A-C		H.-J. Wunderlich and G. Kiefer. Bit-Flipping BIST. In <i>Proceedings VLSI Testing Symposium</i> , pages 337-343, 1996.	
S-A-C		H.-J. Wunderlich. Multiple Distributions for Biased Random Test Patterns. In <i>Proceedings IEEE International Test Conference</i> , pages 236-244, 1988.	
S-A-C		S. Hellebrand. B. Reeb. S. Tarnick. H.-J. Wunderlich. Pattern Generation for a Deterministic BIST Scheme. In <i>Proceedings IEEE International Test Conference</i> , pages 88-94, 1995.	
S-A-C		J. A. Waicukauski. E. Lindbloom. E. B. Eichelberger. O. P. Forlenza. A method for generating weighted random test patterns. IBM J. Res. Develop. Vol. 33. No. 2 March 1989, pages 149-161.	
S-A-C		G. Kiefer and H.-J. Wunderlich. Using BIST Control for Pattern Generation. In <i>Proceedings IEEE International Test Conference</i> , pages 347-355, 1997.	
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S-A-C		On-Chip Bus Attributes. Specification 1 Version 1.0 (OCB 1 1.0) dated August 1998, On-Chip Bus Development Working Group, VSI Alliance.	
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S-A-C		. Savaria. B. Lague. B. Kaminska. A Pragmatic Approach to the Design of Self-Testing Circuits. Electrical Engineering Dept., Ecole Polytechnique de Montreal. In <i>Proceedings IEEE International Test Conference</i> , pages 745-754, 1989.	
S-A-C		H.-C. Tsai. K.-T. Cheng. C.-J. Lin. S. Bhawmik. Efficient Test-Point Selection for Scan-Based BIST. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 6, No. 4, December 1998.	
S-A-C		N. Tamarapalli and Janusz Rajski. Constructive Multi-Phase Test Point Insertion for Scan-Based BIST. In <i>Proceedings IEEE International Test Conference</i> , pages 649-658, 1996.	

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